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Quantum point contact with large subband energy spacings

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Quantum point contact (QPC) with an extra metallic gate in between the split gates of a conventional QPC was fabricated and studied. Clear conductance quantization was observed at 4.2 K when a proper positive voltage was set to the middle gate of the QPC. The maximum energy spacing between the ground and the first exited state of the QPC was around 7 meV which is at least a few times larger than that of conventional QPCs. Using same approach, a possibility of making a relatively clean and long 1D wire has been tested. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4710522]

The conductance quantization at integer multiples of $G_0 = 2e^2/h$ through a narrow constriction was first observed in late eighties.[1,2] The result is the manifestation of ballistic transport of electrons through spin degenerate noninteracting one-dimensional (1D) channel. Soon after the observation of the conductance quantization, unusual quantization phenomenon so called "0.7 structure"[3] has been observed which cannot be explained by a single-particle picture. Extensive research has been done to explain this unusual phenomenon.[4,5] Despite of numerous works performed on 0.7 structure, not much effort was focused on increasing the operation temperature of QPC itself, except for the works performed by Kristensen *et al.*[6,7]

For practical purpose, it is quite important to develop a quantum point contact (QPC) that shows a reasonable conductance quantization at temperature of 4.2 K or above. A conventional QPC employs a split-gate to squeeze 2-dimensional electron gas (2DEG) electrostatically to make a short quasi 1D conduction channel. Such QPC rarely shows reasonable conductance quantization at 4.2 K. Kristensen *et al.* developed a new kind of QPC which is a short 1D wire, prepared by etching 2DEG, with a metallic gate across the wire.[6,7] Remarkably, they have observed a clear conductance quantization at around 4.2 K and above. Despite of a very high working temperature, there are crucial limits for this type of QPCs. Since the QPC is based on etched 1D wire, it is difficult to couple the QPC with other quantum structures like quantum dot, electron interferometer, and so on. Also, the device properties are very sensitive to the surface states formed on the walls of etched mesa due to the random distribution of surface states. To achieve high temperature operation without such problems, we propose a new QPC structure with an extra gate in the gap of a conventional QPC. Similar structure has been used to change the electron density of a 1D wire to study the electron correlation in the wire,[8] but no effort was focused on increasing the subband energy spacings.

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Figure 1 shows the schematic concept of increasing the subband energy spacings in our "3-gate QPC" device. Typically, a conventional QPC has around 300 nm gap between the gates of a QPC and the 2DEG lies around 100 nm below the surface of the heterostructure. In a conventional QPC, the potential on the channel is not zero due to the potential drawn by the nearby QPC gates. Hence, the potential on the channel is lifted above the conduction band minimum. This makes the potential profile of the 1D channel shallow and broad to give rather small subband energy spacings. To avoid unwanted potential lift on the channel, an extra gate is placed in the gap of our 3-gate QPC. As it is shown in Fig. 1(b), a positive voltage applied on the gate will lower the potential of the channel and make a potential profile deep and sharp. This will make subband energy spacings larger than those of a conventional QPC.

The QPC was fabricated on a conventional uniform doped GaAs/GaAlAs heterostructure grown by molecular beam epitaxy (MBE). The 2DEG is buried 77 nm below the surface of the $GaAs/Al_{0.34}Ga_{0.66}As$ heterostructure. The carrier density was $1.9 \times 10^{11}\ cm^{-2}$, and the mobility was $1.1 \times 10^6\ cm^2/Vs$ at 4.2 K in temperature. The 3-gate QPC structure was defined by using electron beam lithography, and 15/30 nm thick Ti/Au was used for the gates. Three types of QPCs, which are different in size, were fabricated. All the QPCs look similar to the one shown in the Fig. 1(c). Only the width of the middle gate and the gap between QPC gates and the middle gate are varied. The length of QPC gate was fixed to 200 nm while varying the width of the middle gate to 50 nm, 75 nm, and 100 nm. The gaps between middle gate and two gates defining QPC were kept the same as the width of the middle gate. For example, a device with 50 nm-wide middle gate has 50 nm gap between nearby gates. All the measurements were carried out at temperature of 4.2 K in liquid helium. The conductance $G = dI_{sd}/dV_{sd}$ was measured with an excitation voltage of $100\ \mu V_{rms}$, using standard lock-in technique.

Figure 2 shows the quantization of conductance observed at 4.2 K in temperature. The conductance was measured as a function of QPC gate voltages, while varying the middle gate voltages. The first curve on the right was

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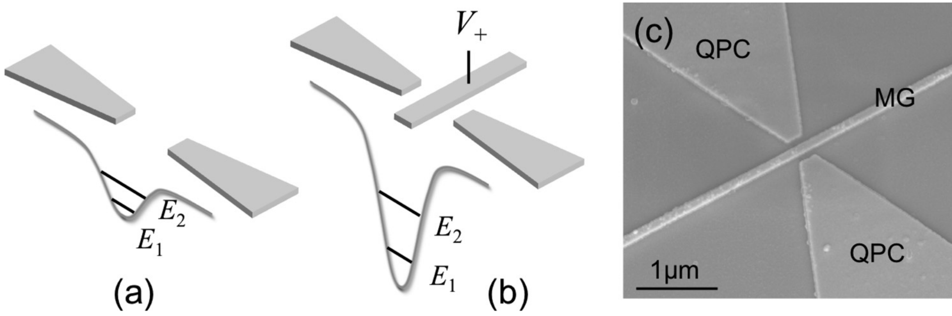

FIG. 1. The schematic concept of increasing the subband energy spacings in a "3-gate QPC" device. The schematic diagram of (a) a conventional QPC and its potential profile and (b) a 3-gate QPC and its potential profile. By adjusting the voltages on the QPC gate and the middle gate, the potential profile and the depth of the conducting channel can be controlled. (c) The SEM picture of a 3-gate QPC device.

measured when the middle gate voltage was set to 0.3 V. At this middle gate voltage, conductance quantization starts to appear while almost no quantization was observed for the middle gate voltages below 0.3 V. As the middle gate voltage is increased, the conductance quantization become clearer, and the width of the plateaus become wider. When the middle gate voltage is higher than 0.7 V, the width and the flatness of the plateaus stay pretty the same. Notice that the quantized plateaus are fully developed and clearly distinguishable. The result is comparable to the results measured with conventional QPCs at temperature below a few hundred mK. The increase in middle gate voltage shifts the pinch-off voltage to more negative value until the middle gate voltage reaches around 0.9 V. Around this voltage, the middle gate starts to leak to the 2DEG dramatically, and the gating is no longer effective. To measure the subband energy spacings, the differential conductance traces $G(V_{QPC})$ were measured for various fixed source-drain voltages V_{sd}. Figure 3(a) shows the grey-scale plot of the transconductance traces dG/dV_{QPC} obtained by numerical differentiation of the measured data. The subband energy spacings can be obtained by finding the value of eV_{sd} at the first intersections of the light straight lines (dotted lines in the figure).[9] For a QPC with 100 nm-wide middle gate, the first subband energy spacing $(E_2 - E_1)$ was around 7 meV while $(E_3 - E_2)$ and $(E_4 - E_3)$ were around 5 meV and 4 meV when the middle gate voltage was set to 0.85 V. Note that the largest energy spacing $(E_2 - E_1)$, reported for a conventional QPC, is around 3 meV.[9]

Figure 3(c) shows the dependence of the first subband energy spacing $(E_2 - E_1)$ on the middle gate voltage. Two different types of devices (50 and 100 nm wide middle gate devices) were used for the measurements. Below 0.75 V in middle gate voltages, the subband energy spacing increases monotonically as the middle gate voltage is increased. This clearly shows that the middle gate can control the subband energy spacing directly. Above 0.75 V in middle gate voltages, the first subband energy spacings saturate to 7 meV for both 50 nm and 100 nm middle gate devices, even though the device with 50 nm middle gate has the QPC gap of 150 nm, which is the half of the gap of the device with 100 nm middle gate. All the devices tested show around 7 mV of the first subband energy spacing, irrespective of their gap size, implying similar electro-static potential profiles in the 1D channel. From Fig. 3(c) we see that the subband energy

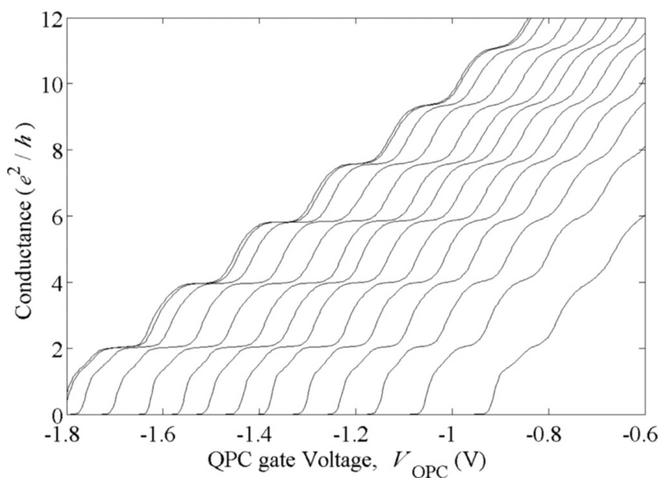

FIG. 2. The conductance through a 3-gate QPC as a function of QPC gate voltage at different middle gate voltages. The middle gate voltage was varied from 0.3 V to 0.95 V in the steps of 0.05 V (right to left). All the measurements were performed at 4.2 K.

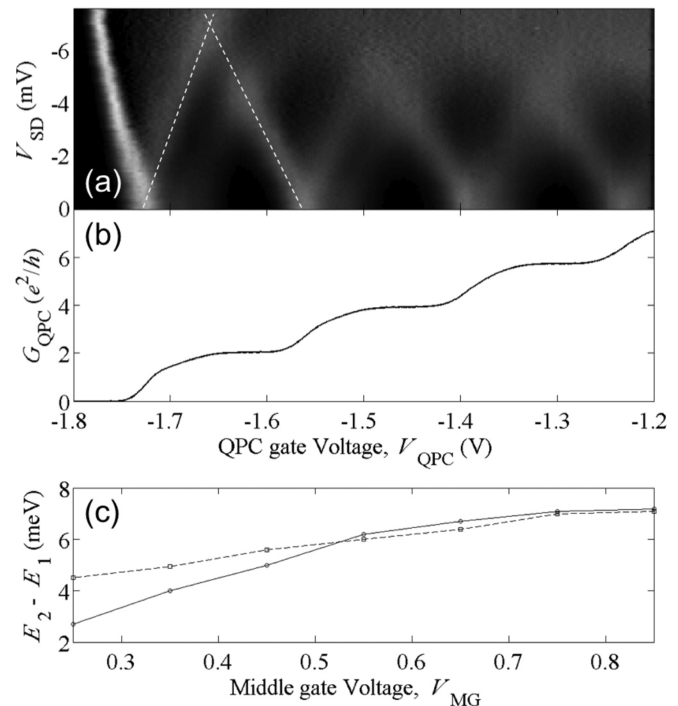

FIG. 3. The differential conductance traces $G(V_{QPC})$ were measured for various fixed source-drain voltages V_{sd}. (a) The grey-scale plot of the transconductance traces dG/dV_{QPC} obtained by numerical differentiation of the measured data. The transconductance is higher for the lighter colors. (b) The conductance measured when the source-drain bias is set to 0 V. (c) The dependence of the first subband energy spacing $(E_2 - E_1)$ on the middle gate voltage for the devices with 100 nm (dashed line) and 50 nm (solid line) wide middle gate.

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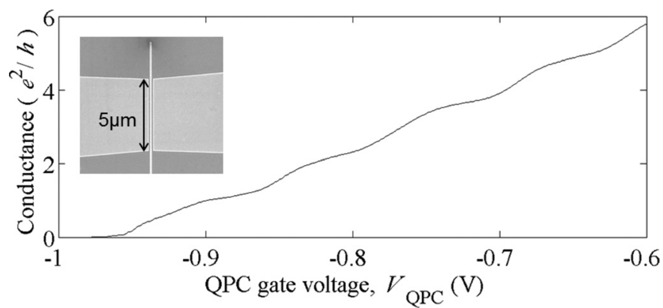

FIG. 4. The conductance quantization measured for a QPC with a 5 μm long channel length. The inset is the SEM picture of the device.

spacing of the 50 nm device, compared to the 100 nm device, shows more sensitive response to the middle gate voltage.

To study the feasibility of creating a clean 1D wire with the same approach, relatively long 1D wires having 1, 2, and 5 μm channel length were fabricated and tested. Usually, it is not so easy to make a clean 1D wire with conventional QPC technique due to local scattering barriers induced by randomly distributed impurity ions in the modulation doped layer. Figure 4 is the conductance quantization measured with a 5 μm long 1D wire with 200 nm wide middle gate and 100 nm gap between QPC gate and the middle gate.

A few quantized conductance plateaus were observed as a function of QPC gate voltage. However, the height of the conductance steps was only around the half of $2e^2/h$ while those of 1 μm long channel device was close to $2e^2/h$. By comparing the results from 1, 2, and 5 μm channel devices, it was found that the height of the step reduces as the length of the channel increases. This cannot be explained by a series resistance (between contacts and a wire) added to the QPC channel resistance. The two-terminal conductance is given by $1/(nG_0 + R_s)$, where R_s is the series resistance and n is the number of channels in the QPC. Hence, the height of the conductance step, measured by two-terminal measurement, decreases as the number of channel in the QPC increases, which is well known. This gives smaller step height between plateaus as the number of channels in the device increases. This is not the case for our device, which gives rather constant step height ($\sim 0.6 \times 2e^2/h$) regardless of the number of channels in the QPC, as it is shown in the figure. Yacoby *et al.*[10] reported conductance step less than unity (0.85) observed in a high quality 1D wire grown by cleaved edge overgrowth. Their values range between 0.8 and 0.9 depending on the well width. Even though our value deviates from the reported value the overall conductance behavior is consistent with their observation. This shows some possibility of creating a clean 1D wire with conventional fabrication process and materials.

In summary, a new type of QPC with additional middle gate, having larger subband energy spacings than those of a conventional QPC, is proposed and tested. Clear conductance quantization was observed at 4.2 K when a proper positive voltage was set to the middle gate of the QPC. We believe that this work show a possibility of creating other various quantum structures which works at liquid helium temperature.

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